

AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 3, line 26 with the following rewritten version:

The data conversion system according to a first aspect ~~claim 1~~ of the present invention is a data conversion system configured so that one of first and second nodes on an IEEE1394 bus serves as cycle master, first data is transferred from the first node to the second node in synchronism with a cycle start packet output from the cycle master, and second data generated by conversion of the first data by the second node is synchronized with an external reference signal and output, and comprises an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes; and a synchronization adjustment unit for synchronizing the cycle start packet frequency output from the cycle master with the frequency of the reference signals received by the external synchronizing signal receiver.

Please replace the paragraph beginning at page 4, line 10 with the following rewritten version:

The data conversion system according to a second aspect ~~claim 2~~ of the present invention is the data conversion system according to the first aspect ~~claim 1~~, wherein the first node is hardware comprising a 1394OHCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data

conversion hardware for outputting an analog video signal or SDI video signal as second data.

Please replace the paragraph beginning at page 4, line 18 with the following rewritten version:

The data conversion system according to a third aspect ~~claim 3~~ of the present invention is the data conversion system according to the first aspect ~~either one of claim 1 or claim 2~~, wherein the second node has an external synchronizing signal receiver and synchronizing adjustment unit, and serves as cycle master for data transfer.

Please replace the paragraph beginning at page 4, line 24 with the following rewritten version:

The data conversion system according to a fourth aspect ~~claim 4~~ of the present invention is a data conversion system according to the first aspect ~~either one of claim 1 or claim 2~~, wherein the first node has a synchronization adjustment unit, the second node has an external synchronizing signal receiver and synchronization adjustment unit, and the synchronization adjustment unit of the node serving as cycle master synchronizes the cycle start packet frequency with a reference signal received by the external synchronizing signal receiver.

Please replace the paragraph beginning at page 5, line 3 with the following rewritten version:

The data conversion system according to a fifth aspect ~~claim 5~~ of the present invention is the data conversion system according to the fourth aspect ~~claim 4~~, wherein when the first node serves as cycle master, the synchronizing adjustment signal generated in accordance with the reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of the IEEE1394 interface.

Please replace the paragraph beginning at page 5, line 12 with the following rewritten version:

The data conversion system according to a sixth aspect ~~claim 6~~ of the present invention is a data conversion system according to the fourth aspect ~~claim 4~~, comprising a dedicated synchronization signal line for transmitting, from the second node to the first node, the synchronizing adjustment signal generated in accordance with the reference signal received by the external synchronizing signal receiver of the second node, the transmission performed in situations in which the first node serves as cycle master.

Please replace the paragraph beginning at page 5, line 21 with the following rewritten version:

The data conversion system according to a seventh aspect ~~claim 7~~ of the present invention is the data conversion system according to the first aspect ~~either one of claim 1 or claim 2~~, wherein the first node has an external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer.

New-(National Phase of PCT/JP2003/011949)
Preliminary Amendment

Please replace the heading at page 6, line 5 with the following rewritten version:

Preferred Embodiments Of The Invention ~~Best Mode to Carry Out the Invention~~

Please replace the sentence at page 12, line 1, with the following rewritten version:

What Is Claimed Is: ~~Claims~~